State-of-the-Art 60 GHz, 3.6 K-Ohm Transimpedance Amplifier for 40 Gb/s and Beyond

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Abstract — A 3.6 K-Ohm InP HBT transimpedance amplifier (TIA) has been demonstrated with a bandwidth of 60 GHz. Gain flatness of +/- 2 dB and dc power of 271 mW has also been obtained. This TIA benchmarks the best gain-bandwidth product (GBP) of 1.9 THz, the highest transimpedance-bandwidth product (TZ-BWP) of 216 Ohm-THz, and the highest TZ-BWP per dc power efficiency of +797 Ohm-GHz/mW obtained for a 40 Gb/s transimpedance amplifier. These results will be discussed in context with prior state-of-the-art 40 Gb/s TIAs implemented with various technologies and circuit topologies. 40 Gb/s photo-receiver requirements, TIA technology and topology trades, and future directions will be reviewed.

INTRODUCTION

At 40 Gb/s, photo-receiver performance is dependent on several factors: (1) photo diode optical and electical performance such as responsivity, carrier transit time limit, and RC electrical parasitics, (2) transimpedance amplifier semiconductor performance such as gain, noise, overload, and bandwidth, and (3) integration parasitics such as series input inductance and stray capacitance. While the photo diode technology sets the physical limit on sensitivity and bandwidth performance in a receiver, the choice of TIA technology and design approach strongly determines overall receiver performance.

In this presentation we will review 40 Gb/s TIA requirements and current state of the art performance, discuss TIA semiconductor technology and design trades, and reveal a new benchmark published for the first time.

I. 40 GB/S PHOTO-RECEIVER AND TIA REQUIREMENTS

Fig. 1 gives the general 40 Gb/s receiver and TIA requirements. A target for optical input sensitivity is less than -10 dBm with a goal of -14 dBm and a photo-receiver bandwidth anywhere from 30 to 50 GHz, depending on the application. This typically requires photo-diode responsivities of > 0.5 A/W with bandwidths > 50 GHz. Presently only InGaAs edge illuminated photo-diodes whose transit time and responsivity can be optimized independently satisfy these requirements, just out of reach
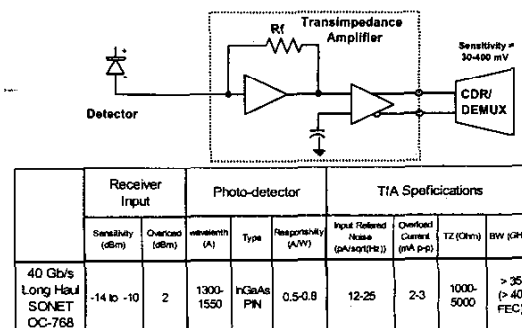

Fig. 1– 40 Gb/s Photo-receiver and TIA requirements.

	Receiver Input		Photo-detector			TIA Spetications			
	Sensitivity (dBm)	Overload (dBm)	wavelength (λ)	Type	Responsivity (A/W)	Input Referred Noise (pA/sqrt(Hz))	Overload Current (mA p-p)	TZ (Ohm)	BW (GHz)
40 Gb/s Long Haul SONET OC-768	-14 to -10	2	1300-1550	InGaAs PIN	0.5-0.8	12-25	2-3	1000-5000	> 35 (> 40 FEC)

of vertical PIN diodes structures. Waveguide photo-diodes (WGPD) with edge-illuminated structures are also developed for a monolithic PIN-TIA integration approach but assumes higher process complexity and cost.

The TIA noise requirements can be derived from PIN responsivity and receiver sensitivity requirements. The TIA requires an input referred noise current of between 12-25 pA/sqrt(Hz). TIA gain is determined by receiver optical sensitivity and the electrical CDR/DEMUX input sensitivity levels. TIA gain of between 1000 and 5000 ohms will typically be required and is strongly dependent on how the limiter post amplifier gain is partitioned. For a CDR/DEMUX's with an integrated limiter, sensitivity as low as 30 mVpp are attainable while those without a limiter can be as high as 400 mVpp. Depending on the semiconductor technology used, it may be more efficient to partition more limiter gain with the TIA.

The bandwidth of the TIA must be at least 35 GHz for NRZ applications when considering electrical module losses, integration parasitics, and transit time limitations of the photo-diode. For RZ modulated data, FEC, and instrumentation applications it is desireable to have photo-RX bandwidths of > 40 GHz which imposes even higher TIA bandwidth requirements. Presently, bandwidth, gain and low dc power are a premium when considering 40 Gb/s TIAs.
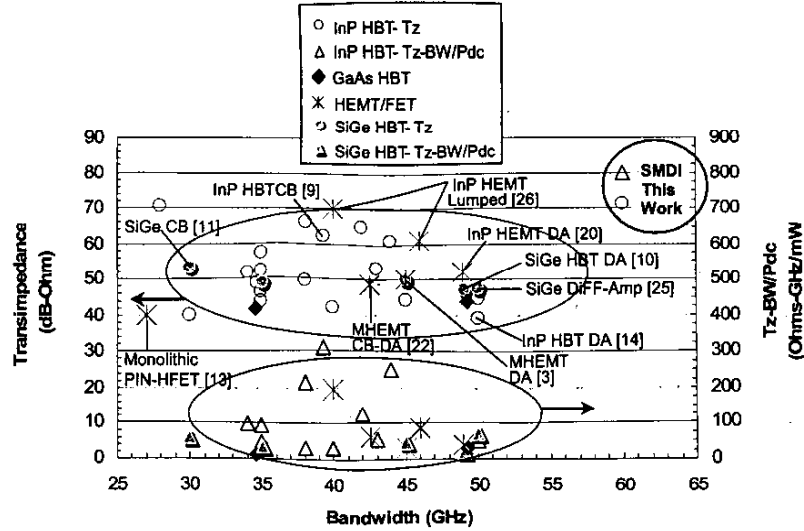
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Figure 1 – Summary of State-of-the-art 40 Gb/s transimpedance amplifiers [1]-[27] including this work.

Technology	Ft	TZ	DC Power	Input Referred Noise	Tz-BW/Pdc	Tz-BWP	DIFF OUT	Comments
	GHz	ohms	mW	pA/sqrt (Hz)	Ohm-GHz/mW	THz		
InP HBT $$$	120-175	450-3,300 3600	150-600	15-20	100-300 +797	50-75 216	YES	Highest TZ, Tz-BWP, and TZ Efficiency, Lowest Noise
InP HEMT $$$$	130, 167	400-560 2250-3170	500-650	-	40-100 195	20-63 127	NO/YES	OK Performance, Not Easily Integrated
MHEMT $$	150	250-300	180-460	15-25	30-60	10-15	NO	LOW COST 6" MHEMT
SiGe HBT $	100-130 200	220-460	200-300 520	15-30	35-70	10-15	YES	Not DC efficient
GaAs HBT $$	100	120-160	250-350	20	12-30	4-8	NO	Poor Performance

Table I- Summary of 40 Gb/s TIAs by technology.

II. STATE OF THE ART 40 GB/S TIA PERFORMANCE

Fig. 1 gives a summary of previously reported 40 Gb/s transimpedance amplifiers reported to date [1]-[27]. Note that only publications which disclose transimpedance-bandwidth or O-E responses are included in this summary. Transimpedance (left axis) is plotted vs. bandwidth while the transimpedance-bandwidth-product per dc power figure of merit is plotted on the right Y-axis. This figure of merit (FOM) measures the efficiency by which a TIA can provide gain and bandwidth and is both design and technology dependent. This FOM becomes important as more hardware is required for the deployment of WDM and DWDM systems which utilize multiple wavelengths to increase transmission capacity.

By inspection of figure 1, it is clear that the InP HBT TIA of this work (SMDI) achieves the best transimpedance (3.6 K-Ohms or 71.1 dB-Ohm) and bandwidth (60 GHz) so far reported for a 40 Gb/s TIA design. Other designs also achieving > 45 GHz bandwidth and built in a variety of technologies include an InP HEMT DA [20], a SiGe HBT DA and differential amp [10,25], an InP HBT DA [14], and a conventional GaAs HBT CE TIA [12]. Note that most are distributed designs, however they all fall short of the SMDI InP HBT lumped topology design of this work by over an order of magnitude (15 dB) in gain and/or 10 GHz in bandwidth. Moreover, the transimpedance-bandwidth product (Tz-BWP) and Tz-BWP per dc power efficiency figure of merit of 216 Ohm-THz and 797 Ohm-GHz/mW respectively, are the best so far reported surpassing the previous record of 127 Ohm-THz and 195 Ohm-GHz/mW demonstrated by an InP HEMT lumped element differential output design by Fujitsu [26].

Other conclusions about TIA technologies can be drawn from the summary in Table I. By inspection, we can conclude that the InP HBT based TIAs generally achieve the best transimpedance-bandwidth and dc efficiencies relative to other technologies. This is mainly due to the high transconductance offered by HBTs, fundamentally a bipolar device, which has 6-10 times the transconductance

compared to a HEMT or FET device operating at the same bias current. However, HEMT technologies can attain even greater bandwidths using distributed topologies due to their low input depletion capacitance compared to the high diffusion capacitance of HBTs, but this is usually at the expense of lower gain (gm) and single-ended output operation. SiGe 40 Gb/s TIAs typically demonstrate less than 500 ohms of transimpedance gain and are less dc efficient than InP HBTs by an order of magnitude, partly due to their much lower fmax which is fundamentally limited by the higher base sheet resistance of SiGe BJT devices. Thus it may be more efficient to integrate the limiter gain into an InP TIA than into a SiGe CDR/DEMUX circuit. It is also interesting to note that about 70-80% of the commercially developed 40 Gb/s TIAs are based on InP technology, a conscious choice made by many fabless 40 Gb/s start-ups.
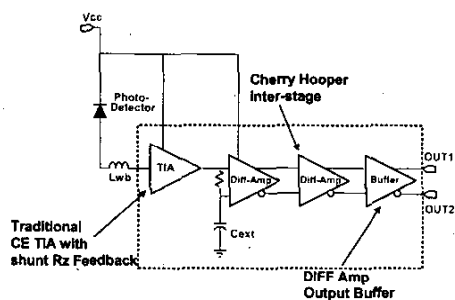

Fig. 2 – Schematic of the InP HBT TIA Design.

III.   BENCHMARK: 3.6 K-OHM, 60 GHz INP HBT TIA

The InP HBT transimpedance amplifier of this work was fabricated using GCS InP SHBT technology. The transistors have fT and fmax of 150 GHz and > 200 GHz respectively, at a conservative current density of 1 mA/um². Typical DC current gain (Beta) and breakdown voltage (BVceo) are 30 and 3-3.5V, respectively.

Fig. 2 gives a block diagram of the circuit schematic. The TIA consists of a conventional common-emitter transimpedance pre-amplifier followed by two Cherry Hooper differential amplifier stages and a 50 ohm differential output buffer stage. The TIA also integrates proprietary DC compensation and dynamic offset control functions to improve dynamic range, as well as photo-current monitor. All the HBT transistors are biased at or below a conservative current density of 0.8 mA/um² in order to insure reliable operation. The TIA is self-biased at 3.3V and draws 82 mA for a total power consumption of about 271 mW. Fig. 3 shows a microphotograph of the InP HBT TIA. The chip size is 1x1mm² and is 100 um thick.
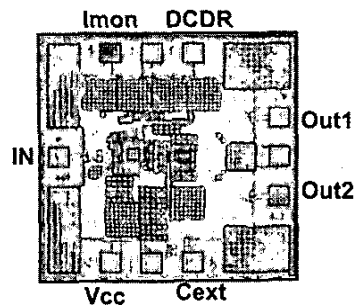

Fig. 3 – Microphotograph of the 60 GHz InP HBT TIA. Chip size is 1x1mm².

Fig. 4 gives the small-signal S-parameters of the InP HBT TIA. The gain is 30 dB with a bandwidth of 60 GHz. The gain flatness is within +/- 2 dB across the 60 GHz band. The input and output return-losses are better than 15 dB and 10 dB up to 40 GHz, respectively.

The calculated gain-bandwidth product (GBP) is greater than 1.9 THz which is 34% higher than the previous state-of the-art obtained by an InP HEMT lumped element pre-amplifier [26] and 36% better than the best GBP demonstrated by a directly cascaded two-stage distributed amplifier built in InP HBT technology [27].
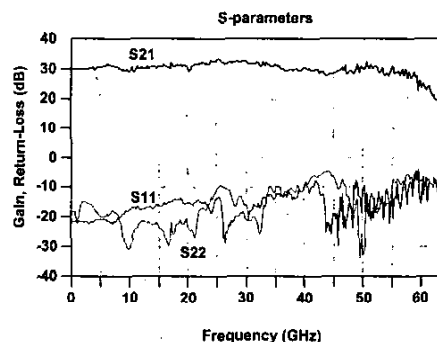

Fig. 4 – S-parameters of the 60 GHz InP HBT TIA.

The transimpedance-bandwidth response was calculated from these S-parameters while also incorporating a typical 40Gb/s InGaAs PIN model which includes a diode parasitic capacitance of 50 fF, contact resistance of 15 ohms, inductive trace of 0.1 nH, pad shunt parasitic capacitance of 15 fF, and series ribbon interconnect inductance of 0.15 nH which connects the PIN die to the TIA die. The resulting response yields a differential transimpedance of 71.1 dB-Ohm (or 3.6 K-Ohms) with a 3 dB bandwidth of 60 GHz given in Fig. 5. As mentioned

before, the Tz-BWP and Tz-BWP/Pdc FOM are 216 THz and +797 Ohm-GHz/mW, respectively, and benchmark the highest reported to date.

Fig. 6 gives the error-free eye diagram of VSK Photonics 40 Gb/s photo-receiver which integrates a lower gain (2000 ohm) version of the TIA of this paper. The optical input power is -10 dBm. Estimated sensitivity is between -12 and -14 dBm based on worst case 20 pA/sqrt(Hz) TIA noise measurement. Measured receiver bandwidth is > 50 GHz and is believed to be best in class performance with 1000 V/W conversion gain. Higher receiver gain, bandwidth and similar noise is expected from the 3.6K-ohm TIA of this paper.
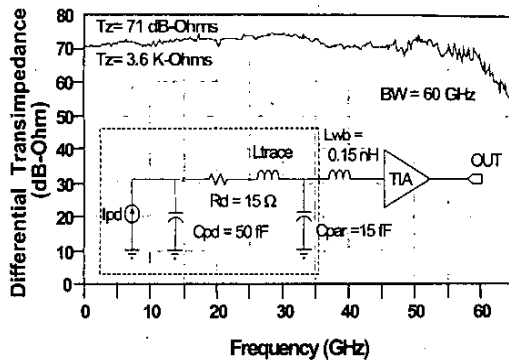

Fig. 5 – Transimpedance response based on TIA S-parameters incorporating photo-detector and interconnect parasitics.
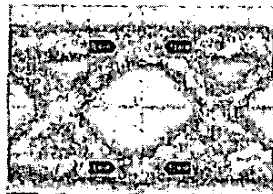

Fig. 6 – 40 Gb/s Error Free Eye Diagram of VSK Photonic's photo-receiver integrating SIRENZA's (low gain version) TIA with a Pin = -10 dBm.

IV.   FUTURE DIRECTIONS

Lumped element design combined with high speed InP HEMT and HBT technologies appear to be the preferred approaches for 40 Gb/s TIA Applications. DPSK balanced photo-receivers with improved SNR is on the horizon and is an excellent match with the high speed analog bipolar characteristics of InP HBTs. For 80 Gb/s NRZ operation, the InP HBT lumped TIA design of this work is adequate, however, 80 Gb/s RZ and beyond may require a combination of lumped element and distributed design

techniques that are more suitable with low input capacitance devices such as InP HEMT and GaAs MHEMT technologies. Emerging sub-micron InP HBT will also be a candidate using a hybrid of lumped and distributed approaches.

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